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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,517	12/11/2003	Gernot Eckstein	S0193.0011	1592

38881 7590 11/05/2008

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EXAMINER	
JOHNSON, CARLTON	
ART UNIT	PAPER NUMBER
2436	

MAIL DATE	DELIVERY MODE
11/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/735,517	ECKSTEIN ET AL.	
	Examiner	Art Unit	
	CARLTON V. JOHNSON	2436	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responding to application amendments filed on 7-17-2008.

2. Claims **1, 3, 5 - 10** are pending. Claims **1, 3, 6** have been amended. Claims **1, 3** are independent. This application was filed on 12/11/2003.

Response to Remarks

3. The following is in response to papers dated 7-17-2008. Applicant's arguments have thus been fully considered but they were not persuasive.

3.1 Applicant argues, "to replace Niessen's feedback of the filling degree signal with a random generator or with a signal varying the supply voltage in a random way". (see Remarks Page 5)

Niessen discloses that the voltage varies as a factor of time. Varying the voltage in a random way does not negate the fact that the voltage varies based on time just the frequency of the time signal. The inclusion of Dias discloses that the voltage varies in a random manner. A 103 rejection discloses the combination of concepts. The 103 combination of Niessen and Dias proposes the inclusion of the random number generation feature of Dias and using the concept of this feature to control the timing of voltage within the already established features or limitations of the Niessen invention. Even with a random signal as the filling degree signal the filling should still occur. There was no suggestion of replacing the Niessen circuit with a random number generator.

There is no indication that the desired filling-degree control of Niessen would no longer work. (see Remarks Page 5)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, **3, 5, 7, 9, 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Niessen et al.** (US patent No. **5,367,638**) in view of **Dias** (US Patent No. **4,855,690**).

Regarding Claim 1, Niessen discloses a method of preventing the external detection of operations in a digital integrated circuit comprising an asynchronous circuit (see Niessen col. 3, lines 65-68: asynchronous circuit (integrated circuit)), comprising time-varying a supply voltage (see Niessen col. 1, lines 26-28: self timed circuit varies supply voltage; col. 8, lines 56-60: vary the supply voltage to said electronic circuitry; speed up operation of circuit) of said asynchronous circuit to time-shift the execution time of operations within said asynchronous circuit. (see Niessen col 1, lines 58-63: powering voltage directly determines the operating speed of said electronic circuitry)

Niessen discloses wherein a time variation of said supply voltage. (see Niessen col. 5,

lines 4-8: regulating the output of a varying voltage source varying of voltage; col. 8, lines 56-60: vary the supply voltage to said electronic circuitry) Niessen does not specifically disclose that time variation takes place in a random way. However, Dias discloses wherein the time variation of said supply voltage takes place in a random way. (see Dias col. 1, lines 53-58: generate random numbers in which a time varying voltage is generated)

It would have been obvious to one of ordinary skill in the art to modify Niessen for time variation to take place in a random way as taught by Dias. One of ordinary skill in the art would have been motivated to employ the teachings of Dias in order to enable a random number generator which produces random numbers on a relatively small area of an integrated circuit. (see Dias col. 1, lines 31-34: *" ... Therefore, it can be appreciated that a random number generator circuit which produces random numbers on a relatively small area of an integrated circuit is highly desirable. ... "*)

Regarding Claim 3, Niessen discloses a digital integrated circuit comprising: an asynchronous circuit, and means for time-varying a supply voltage of said asynchronous circuit to time-shift the execution point of operations within said asynchronous circuit. (see Niessen col. 3, lines 65-68: asynchronous circuit; col. 5, lines 4-8: regulating the output of a varying voltage source varying of voltage; col. 8, lines 56-60: vary the supply voltage to said electronic circuitry)

Niessen discloses wherein a time variation of said supply voltage. (see Niessen col. 5, lines 4-8: regulating the output of a varying voltage source varying of voltage; col. 8,

lines 56-60: vary the supply voltage to said electronic circuitry) Niessen does not specifically disclose a random number generator. However, Dias discloses wherein said means for time-varying said supply voltage comprising a random number generator. (see Dias col. 1, lines 53-58: method for random number generation random numbers)

It would have been obvious to one of ordinary skill in the art to modify Niessen a random number generator as taught by Dias. One of ordinary skill in the art would have been motivated to employ the teachings of Dias in order to enable a random number generator which produces random numbers on a relatively small are of an integrated circuit. (see Dias col. 1, lines 31-34)

Regarding Claim 5, Niessen discloses the digital integrated circuit according to claim 4, wherein said means for time-varying said supply voltage. (see Niessen col. 5, lines 4-8: regulating the output of a varying voltage source varying of voltage; col. 8, lines 56-60: vary the supply voltage to said electronic circuitry) Niessen does not specifically disclose a noise voltage source driving said random-number generator. However, Dias discloses wherein further comprising a noise voltage source driving said random-number generator. (see Dias col. 1, lines 53-58: method for generation of random numbers)

It would have been obvious to one of ordinary skill in the art to modify Niessen for a noise voltage source driving said random-number generator as taught by Dias. One of ordinary skill in the art would have been motivated to employ the teachings of Dias in

order to enable a random number generator which produces random numbers on a relatively small are of an integrated circuit. (see Dias col. 1, lines 31-34)

Regarding Claim 7, Niessen discloses the digital integrated circuit according to claim 3, wherein said means for time-varying said supply voltage further comprises a voltage regulator. (see Niessen col. 5, lines 2-4: supply voltage is regulated to actual powering voltage by voltage regulator)

Regarding Claims 9, 10, Niessen discloses the method according to claims 1 and 3, wherein the asynchronous circuit is a type, which performs processing without correlation to a clock. (see Niessen col. 3, lines 65-68: asynchronous circuit; col. 1, lines 26-28: self timed circuit; needs no clock synchronization)

6. Claims **6, 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Niessen-Dias** and further in view of **Read et al.** (US Patent No. **5,353,243**).

Regarding Claim 6, Niessen discloses the digital integrated circuit according to claim 4, wherein said means for time-varying said supply voltage. (see Niessen col. 3, lines 65-68: asynchronous circuit (integrated circuit); col. 5, lines 4-8: regulating the output of a varying voltage source varying of voltage; col. 8, lines 56-60: vary the supply voltage to said electronic circuitry) However, Dias discloses wherein a random-number generator. (see Dias col. 1, lines 53-58: generate random numbers in which a time

varying voltage is generated)

It would have been obvious to one of ordinary skill in the art to modify Niessen for a random-number generator as taught by Dias. One of ordinary skill in the art would have been motivated to employ the teachings of Dias in order to enable a random number generator which produces random numbers on a relatively small are of an integrated circuit. (see Dias col. 1, lines 31-34)

Niessen-Dias does not specifically disclose a digital-analog converter transforming the digital values into an analog voltage. However, Read discloses wherein a digital-analog converter transforming the digital values into an analog voltage. (see Read col. 25, lines 29-31: reference voltages are supplied by a digital to analog converter)

It would have been obvious to one of ordinary skill in the art to modify Niessen for a digital-analog converter transforming the digital values into an analog voltage as taught by Read. One of ordinary skill in the art would have been motivated to employ the teachings of Read in order for systems used by electronics designers to simulate the operation of electronic circuits during development and testing of electronic systems including circuits to combat attacks on integrated circuits. (see Read col. 1, lines 11-10: *" … The present invention relates to systems used by electronics designers to simulate the operation of electronic circuits during development and testing of electronic systems. More specifically, the invention relates to hardware modeling systems that use examples of actual physical electronic circuits and components to model their behavior within a simulated electronic system design. … "*)

Regarding Claim 8, Niessen discloses the digital integrated circuit according to claim 3, wherein said asynchronous circuit. (see Niessen col. 5, lines 4-8: regulating the output of a varying voltage source varying of voltage; col. 8, lines 56-60: vary the supply voltage to said electronic circuitry) Niessen does not specifically disclose executing a coding algorithm. However, Read discloses wherein formed for executing a coding algorithm. (see Read col. 1, lines 34-36: using code written in an algorithmic language such as "C")

It would have been obvious to one of ordinary skill in the art to modify Niessen for executing a coding algorithm as taught by Read. One of ordinary skill in the art would have been motivated to employ the teachings of Read in order for systems used by electronics designers to simulate the operation of electronic circuits during development and testing of electronic systems including circuits to combat attacks on integrated circuits. (see Read col. 1, lines 11-10)

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlton V. Johnson whose telephone number is 571-270-1032. The examiner can normally be reached on Monday thru Friday , 8:00 - 5:00PM EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nasser G Moazzami/
Supervisory Patent Examiner, Art Unit 2436

Carlton V. Johnson
Examiner
Art Unit 2436

CVJ
October 27, 2008